PATENT APPLICATION
Docket No. 2522-026
Client No. AW8116US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s):	Ji-Young KIM and Hyoung-Sub KIM	Conf. No.	7198
Serial No.:	10/649,262	Examiner:	Not yet assigned
Filing Date:	August 26, 2003	Group Art Unit:	2812
Title:	INTEGRATION METHOD OF A SEMICONDUCTOR DEVICE HAVING A RECESSED GATE ELECTRODE		

INFORMATION DISCLOSURE CITATION
FORM PTO-1449 (Modified)

U.S. PATENT DOCUMENTS

Exam Init	Ref	Document Number	Issue Date	Name	Class	Sub Class
WL		6,063,669	May 16, 2000	Takaishi		
WL		US 2003/0003651 A1	January 2, 2003	Divakaruni, et al.	1	1
WL		US 2003/0011032 A1	January 16, 2003	Umebayashi		

Examiner: WL

Date Considered: 5/11/05

PATENT APPLICATION

In re application of:	Ji-Young Kim and Hyoung-Sub Kim		
Serial No.	Not yet assigned	Examiner:	Not yet assigned
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INFORMATION DISCLOSURE CITATION
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Exam Init	Ref	Document Number	Issue Date	Name	Class	Sub Class
WLC	____	6,063,669	5/16/2000	Takaishi	—	—

FOREIGN PATENT DOCUMENTS

Exam Init	Ref	Document Number	Publication Date	Country	Name
____	____				

OTHER DOCUMENTS

Exam Init	Ref	Author, Title, Date, Pertinent Pages, Etc.)

Examiner: Walter Lindsay

Date Considered: 5/11/05